REMARKS

This is a full and timely response to the outstanding final Office Action mailed November 18, 2004. Reconsideration and allowance of the application and pending claims are respectfully requested.

In the outstanding Office Action, the Examiner reiterates the rejections made in the previous Office Action (mailed July 27, 2004) and provides responses to Applicant's arguments provided in Applicant's previous Response (mailed September 23, 2004). Applicant incorporates the arguments presented in the previous Response and provides replies to the Examiner's Response to Arguments contained in the outstanding Office Action.

I. "Having No Erasing Circuitry"

A. The Widdershoven Disclosure

In Applicant's previous Response, Applicant noted that Widdershoven does not disclose or suggest a high-density non-volatile fast memory "having no erasing circuitry" and that, to the contrary, Widdershoven teaches the opposite: photodiodes that contribute to the erasure of the memory cells to prevent under-erasure of the memory cell.

In response to Applicant's arguments, the Examiner acknowledges that Widdershoven's photodiodes 12 are used to "prevent under erasure during UV irradiation," but argues that Widdershoven teaches that the photodiodes do not perform any erasure and, therefore, that the photodiodes are not erasing circuitry.

Applicant respectfully asserts that the Examiner's argument makes no sense. First, if the photodiode is used to prevent under erasure (i.e., helps the erasure process), it cannot be said that the photodiode does not perform any erasure. Indeed, the whole

purpose for the addition of the photodiodes is to aid in the erasure process. Given that the photodiodes are clearly circuitry, and further given that they perform an erasure function, it logically follows that those photodiodes comprise "erasing circuitry". Therefore, it cannot be said that the Widdershoven device has no erasing circuitry.

As was mentioned in the previous Response, the focus of the Widdershoven disclosure appears to be addition of the photodiodes to assist in memory cell erasure. For example, in the Background of the Invention section of the Widdershoven reference, Widdershoven identifies the problem that must be overcome:

> ***It was found in practice that the threshold voltage often does not return to its original value, for example 1.1 V, during UV erasure, but to a much higher value, for example 2 V.*** This high threshold voltage may give rise to problems in, for example, low-voltage or low-power applications. A memory cell which is programmed in the "ON" state (low threshold) must have a threshold voltage which is substantially lower than the supply voltage. It is indeed possible to generate higher voltages with an on-chip charge pump, but such a charge pump is often not attractive on account of its high dissipation. (Widdershoven, column 1, lines 45-55, emphasis added)

Accordingly, Widdershoven notes that a problem with erasing memory cells with UV radiation is that, in practice, the cell voltage does not return to its original low state (e.g., 1.1 V) after UV exposure. In the Summary of the Invention, Widdershoven describes a solution to the problem. There Widdershoven states the following:

Therefore, ***the invention has for its object to provide, inter alia, a non-volatile, UV-erasable memory in which a lower threshold voltage is obtained during UV-erasure. According to the invention, a semiconductor device of the kind described in the opening paragraph is for this purpose characterized in that means are present for generating a photovoltage during the erasure by means of UV irradiation, which photovoltage is supplied to the control gate.*** The invention is based inter alia on the recognition that in a thermodynamic equilibrium, when the Fermi levels are the same, a built-in voltage is present between the n-type floating gate and the p-type substrate. The n-type floating gate has a potential at room temperature which is approximately 1 V higher than the potential in the substrate in the case of a usual doping level. This potential difference prevents that all electrons applied to the floating gate during writing return to the substrate again during erasing. ***The application of a negative voltage to the control gate during erasing renders it possible to compensate for part of the built-in voltage, so that more electrons will disappear from the floating gate during erasing. The use of a photovoltage generated during the UV irradiation itself as the voltage applied to the control gate renders it unnecessary to use separate, external voltage sources.*** (Widdershoven, column 1, line 58 to column 2, line 14)

From the above excerpt, it is clear that the photodiode, and more particularly the photovoltage that it provides, is used to attain proper erasing that, according to Widdershoven, would not otherwise be possible. Therefore, it is abundantly clear that Widdershoven's photodiodes perform an erasing function, and therefore, comprise erasing circuitry. If the Examiner still disagrees that the Widdershoven photodiodes perform an erasing function, Applicant respectfully requests that the Examiner describe what purpose those photodiodes serve in the Widdershoven device.

In view of the above, Applicant submits that Widdershoven clearly teaches use of erasing circuitry, and that rejection of independent claims 1, 5, 10, 30, and 32, and their associated dependent claims, is clearly unwarranted.

B. The Kazami Disclosure

Independent claims 33 and 35 recite means for erasing "without the use of any erasing circuitry". The Examiner maintains the rejection of those claims in view of the Kazami reference in the outstanding Office Action. Specifically, the Examiner states that Kazami teaches exposing memory to UV light without using any erasing circuitry in column 1, lines 14-18.

In the previous Response, Applicant reproduced column 1, lines 14-18 to reveal what is actually described in that portion of the Kazami reference. Applicant does so again:

> An EPROM element with an ultraviolet light irradiation window provided in its surface by which it is possible to erase stored data written on a chip by ultraviolet irradiation and rewrite into that memory is preferably used in various types of electronic devices.

Although it is true that this portion of the Kazami reference mentions "ultraviolet light irradiation," that portion of the disclosure is woefully deficient in disclosing erasing "without the use of any erasing circuitry". Stated simply, a cryptic reference to UV irradiation does not equate to an explicit teaching of performing such irradiation "without the use of any erasing circuitry".

As was previously mentioned, the above described reference to UV irradiation is description is provided in the Description of the Background Art of the Kazami

reference and, therefore, is not intended to be a complete or "detailed" description of any device as one might find in a Detailed Description section of a patent. Given this fact, the prior art being described by Kazami may or may not include erasing circuitry. Unfortunately, Kazami just does not provide enough information to make that determination.

What is missing in Kazami, and the other prior art of record, is a teaching, whether explicit or inherent, that erasing circuitry is not used. Since no such teaching is supplied by Kazami, the rejection of claims 33 and 35 under 35 U.S.C. § 102 is *per se* improper. Again, anticipation requires the disclosure of *each element* of the claim under consideration." *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983).

II. "Two-Terminal Drain-Gate-Connected Modified Flash Cells"

The Examiner alleges that, contrary to that identified by Applicant in the previous Response, Widdershoven teaches a two-terminal drain-gate-connected modified flash cell. For support, the Examiner states the following:

> Fig. 1 of Widdershoven clearly teaches a modified flash cell (11) by UV light having two terminal drain [2] and gate [3]. Therefore, Widdershoven clearly anticipated the two terminals (drain [2] and gate [3]) comprised by the memory cell of claimed invention.

The above statement is simply false. As a first matter, reference numeral "2" identifies a word line, not a "drain". Widdershoven, column 3, lines 57-59. The drain of the Widdershoven device is identified by reference numeral 8. Widdershoven, column 4, lines 9-10. Second, reference number "3" identifies a bit line, not a "gate".

Widdershoven, column 3, lines 57-59. The control gate of the Widdershoven device is identified by reference numeral 10. Widdershoven, column 4, lines 18-19.

Beyond those errors, it is clear from the Widdershoven disclosure that Widdershoven discloses a three-terminal device, not a two-terminal device. As was described in the previous Response, Widdershoven's device includes the following three terminals: (i) an n-type source 7, (ii) a p-type drain 8, and (iii) a control gate 10. Widdershoven, column 4, lines 4-22.

That Widdershoven does not disclose a two-terminal drain-gate-connected modified flash cell is perhaps best appreciated with reference to Figure 2. If Widdershoven disclosed a two-terminal drain-gate-connected modified flash cell, the drain (8) and the gate (10) would be connected (i.e., short-circuited) together so as to result in two effective terminals: a first terminal (source 7) and a second terminal (drain 8 and gate 10). As is clear from Figure 2, however, each of the source 7, drain 8, and gate 10 are separate from each other. Therefore, Widdershoven teaches a three-terminal device, not a two-terminal drain-gate-connected modified flash cell.

Applicant invites the Examiner to compare what is disclosed by Widdershoven in Figure 2 with Applicant's Figure 1B, which illustrates an example embodiment of a two-terminal drain-gate-connected modified flash cell. As is indicated in Applicant's Figure 1B, the drain 550 is connected to (i.e., short circuited with) the control gate 430 through a line on which a voltage, V_{CD}, is applied. Therefore, the device shown in Figure 1B comprises two terminals: a first terminal comprising the source 630, and a second terminal comprising the drain 550 and the control gate 430.

In view of the above, all rejections based upon the premise that Widdershoven teaches a two-terminal drain-gate-connected modified flash cell are unwarranted and should be withdrawn.

III. "UV Window . . . Located Below a Substrate"

The Examiner also reiterates his position that Widdershoven teaches a UV window located below a substrate. For support, the Examiner argues that Widdershoven shows a UV light window 11 that is located below a substrate 16 in Figure 2.

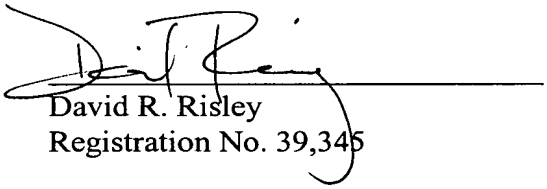
Again, the basis for the Examiner's rejection is false. Although it is true that reference numeral 11 identifies a UV light window, reference numeral 16 identifies a "contact" that joins zone 13 to the control gate 10. Widdershoven, column 4, lines 58-59. Persons having ordinary skill in the art would agree that such a contact simply does not qualify as a substrate. As is well known to such persons, a substrate is a layer of material upon which the various circuits of a device are built upon. Although Widdershoven's reference numeral 16 is not a substrate, Widdershoven does indeed show a substrate: surface region 5 in Figure 2. However, the UV window 11 is clearly above the substrate 5, and not the other way around. See Widdershoven, Figure 2.

As a further point, Applicant notes that, even if reference numeral 16 did identify a substrate (which it clearly does not), the element identified by reference numeral 16 is *beside* the UV light window 11. Therefore, one could not correctly say that the UV light window 11 was "below" the "substrate" 16.

CONCLUSION

Applicant respectfully submits that Applicant's pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,



David R. Risley
Registration No. 39,345

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on

1-5-05

Mary Meegan

Signature